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EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/903,239	CECCHI ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The response filed on 12/18/03 has been received and entered in the case.

Drawings

2. The proposed drawings corrections filed on 01/13/03 were approved in the previous office action (mailed on 3/24/03). Applicant is requested to send in the Replacement drawing sheet(s) including the corrections that were proposed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (USP 6,313,696) in view of Sasaki (USP 5,039,873).

With respect to claim 1, Figure 2 of the Zhang reference discloses a differential amplifier which includes: an active differential amplification circuit (transistors 31, 34, 41-46, 38, and 35 in Figure 2) electrically coupled to a first input signal (ina), a second input signal (inb) and an output signal (out), the active differential amplification circuit (transistors 31, 34, 41-46, 38, and 35) also electrically coupled to a first voltage (Vdd) and a second voltage (GND) different from the first voltage (Vdd); and a bias circuit (transistors 32, 33, 36 and 37 in Figure 2) electrically coupled to the active differential amplification circuit (transistors 31, 34, 41-46, 38, and 35) for biasing the active differential amplification circuit (transistors 31, 34, 41-46, 38, and 35). The

Zhang reference does not teach that the bias circuit (transistors 32, 33, 36 and 37) is a passive circuit. However, the Sasaki reference teaches that when a transistor is on, it is functionally equivalent to a resistor (see Figure 4c, and Col. 1, lines 21-22 of Sasaki). Therefore, because each of the gates of the transistors 32, 33, 36 and 37 of the bias circuit in Figure 2 of the Zhang reference is connected to a respective fixed power supply voltage (Vdd or Gnd) so transistors 32, 33, 36 and 37 will remain on during switching (Col. 7, lines 37-41 of Zhang), it would have been obvious to one having an ordinary skill in the art at the time the invention was made to substitute a resistor for each of the transistors 32, 33, 36 and 37 in Figure 2 of the Zhang reference because they are functionally equivalent and because it is well known in the art that the impedance of the passive resistor is inherently linear (evidence is shown in Col. 5, lines 20-21 of the Stockstad reference, USP 6,429,685). With such a modification, the bias circuit will be a passive bias circuit which includes four resistors. Note that this modification will also meet the functional language "for providing common-mode rejection while providing differential-mode amplification" on lines 1-2 and "the active differential ... the second input signal" on the last 4 lines of the claim because the structure of the modification is the same as the structure of the claimed invention (Figure 2).

With respect to claim 2, the above modification shows that the active differential amplification circuit (transistors 31, 34, 41-46, 38, and 35 in Figure 2 of Zhang) includes: a first transistor (34) having a first source electrically coupled to the first voltage (Vdd), a first gate electrically coupled to a first node (58) and a first drain (connected to node 52), the first node (58) being a bias node; a second transistor (31) having a second drain (connected to node 50), a second gate electrically coupled to the first node (58) and a second source electrically coupled to

the second voltage (GND) different from the first voltage (Vdd); a third transistor (38) having a third source electrically coupled to the first voltage (Vdd), a third drain (connected to node of 56) and a third gate electrically coupled to the first node (58); a fourth transistor (35) having a fourth drain (connected to node 54), a fourth gate electrically coupled to the first node (58) and a fourth source electrically coupled to the second voltage (GND); a fifth transistor (41) having a fifth source electrically coupled to the first voltage (Vdd), a fifth drain electrically coupled to a second node (the junction of transistors 41-43) and a fifth gate electrically coupled to the first node (58); a sixth transistor (44) having a sixth drain electrically coupled to a third node (junction of transistors 44-46), a sixth gate electrically coupled to the first node (58) and a sixth source electrically coupled to the second voltage (GND); a seventh transistor (42) having a seventh source electrically coupled to the second node (junction of transistors 41-43), a seventh drain electrically coupled to the second drain (the connection of transistors 42 and 31 at node 50), and a seventh gate electrically coupled to the first input signal (ina); an eighth transistor (45) having an eighth drain electrically coupled to the first drain (the connection of transistors 45 and 34 at node 52), an eighth source electrically coupled to the third node (junction of transistors 44-46) and an eight gate electrically coupled to the first input signal (ina); a ninth transistor (43) having a ninth source electrically coupled to the second node (junction of transistors 41-43), a ninth gate electrically coupled to the second input signal (inb) and a ninth drain electrically coupled to the fourth drain (the connection of transistors 43 and 35 at node 54); and a tenth transistor (46) having a tenth drain electrically coupled to the third drain (the connection of transistors 46 and 38 at node 56), a tenth gate electrically coupled to the second input signal (inb) and a tenth source electrically coupled to the third node (junction of transistors 45-46).

With respect to claim 3, the above modification also meet the limitation that the passive bias circuit includes: a first resistor (substituted for transistor 33 as discussed above with regard to claim 1) electrically coupling the first drain (node 52) to the first node (58); a second resistor (substituted for transistor 32 as discussed above with regard to claim 1) electrically coupling the second drain (node 50) to the first node (58); a third resistor (substituted for transistor 37 as discussed above with regard to claim 1) electrically coupling the third drain (node 56) to the output signal (out); and a fourth resistor (substituted for transistor 36 as discussed above with regard to claim 1) electrically coupling the fourth drain (node 54) to the output signal (out).

With respect to claim 4, Figure 2 of the Zhang reference shows that the first transistor (34), the third transistor (38), the fifth transistor (41), the seventh transistor (42) and the ninth transistor (43) each include a p-channel device.

With respect to claim 5, Figure 2 of the Zhang reference shows that the second transistor (31), the fourth transistor (35), the sixth transistor (44), the eighth transistor (45) and the tenth transistor (46) each include an n-channel device.

With respect to claim 6, Figure 2 of the Zhang reference shows that second voltage (GND) is electrically coupled to a common ground (GND).

With respect to claim 7, the above modification of Figure 2 of the Zhang reference as discussed in claim 1 also meets all of the limitations of claim 7 because the structure of this modification is the same as the structure of the claimed invention (Figure 2), e.g., the above modification is a differential amplifier which includes: a first transistor (34) having a first source electrically coupled to the first voltage (Vdd), a first gate electrically coupled to a first node (58) and a first drain (connected to node 52), the first node (58) being a bias node; a second transistor

(31) having a second drain (connected to node 50), a second gate electrically coupled to the first node (58) and a second source electrically coupled to a second voltage (GND) different from the first voltage (Vdd); a first resistor (substituted for transistor 33 as discussed above with regard to claim 1) electrically coupling the first drain (node 52) to the first node (58); a second resistor (substituted for transistor 32 as discussed above with regard to claim 1) electrically coupling the second drain (node 50) to the first node (58); a third transistor (38) having a third source electrically coupled to the first voltage (Vdd), a third drain (connected to node of 56) and a third gate electrically coupled to the first node (58); a fourth transistor (35) having a fourth drain (connected to node 54), a fourth gate electrically coupled to the first node (58) and a fourth source electrically coupled to the second voltage (GND); a third resistor (substituted for transistor 37 as discussed above with regard to claim 1) electrically coupling the third drain (node 56) to an output signal (out); and a fourth resistor (substituted for transistor 36 as discussed above with regard to claim 1) electrically coupling the fourth drain (node 54) to the output signal (out); a fifth transistor (41) having a fifth source electrically coupled to the first voltage (Vdd), a fifth drain electrically coupled to a second node (the junction of transistors 41-43) and a fifth gate electrically coupled to the first node (58); a sixth transistor (44) having a sixth drain electrically coupled to a third node (junction of transistors 44-46), a sixth gate electrically coupled to the first node (58) and a sixth source electrically coupled to the second voltage (GND); a seventh transistor (42) having a seventh source electrically coupled to the second node (junction of transistors 41-43), a seventh drain electrically coupled to the second drain (the connection of transistors 42 and 31 at node 50), and a seventh gate electrically coupled to a first input signal (ina); an eighth transistor (45) having an eighth drain electrically coupled to the first

drain (the connection of transistors 45 and 34 at node 52), an eighth source electrically coupled to the third node (junction of transistors 44-46) and an eight gate electrically coupled to the first input signal (ina); a ninth transistor (43) having a ninth source electrically coupled to the second node (junction of transistors 41-43), a ninth gate electrically coupled to a second input signal (inb) and a ninth drain electrically coupled to the fourth drain (the connection of transistors 43 and 35 at node 54); and a tenth transistor (46) having a tenth drain electrically coupled to the third drain (the connection of transistors 46 and 38 at node 56), a tenth gate electrically coupled to the second input signal (inb) and a tenth source electrically coupled to the third node (junction of transistors 45-46). Note that the preamble recitation "for providing common-mode rejection while providing differential-mode amplification" on lines 1-2 is merely intended use.

With respect to claim 8, Figure 2 of the Zhang reference shows that the first transistor (34), the third transistor (38), the fifth transistor (41), the seventh transistor (42) and the ninth transistor (43) each include a p-channel device.

With respect to claim 9, Figure 2 of the Zhang reference shows that the second transistor (31), the fourth transistor (35), the sixth transistor (44), the eighth transistor (45) and the tenth transistor (46) each include an n-channel device.

With respect to claim 10, Figure 2 of the Zhang reference shows that second voltage (GND) is electrically coupled to a common ground (GND).

Response to Arguments

5. Applicant's arguments filed on 12/18/03 have been fully considered but they are not persuasive.

Applicant argues that "the Examiner also recognized 'the advantage of using [a] passive resistor because the impedance of [a] passive resistor inherently is linear.' While, with hindsight, the Examiner recognizes the advantage of the invention, the Examiner has made no statement showing a teaching, suggestion or motivation to combine the Sasaki and Zhang references." In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). Further, in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, because each of the gates of the transistors 32, 33, 36 and 37 of the bias circuit in Figure 2 of the Zhang reference is connected to a respective fixed power supply voltage (the gate of p-channel transistors 33 and 37 connected to ground, and the gate of n-channel transistors 32 and 36 connected to power supply Vdd) so transistors 32, 33, 36 and 37 will remain on during switching (see Col. 7, lines 37-41 of Zhang), so each of the transistors 32, 33, 36 and 37 functions as a resistor since the Sasaki reference teaches that when a

transistor is on, it is functionally equivalent to a resistor (see Figure 4c, and Col. 1, lines 21-22 of Sasaki). Therefore, it is obvious to one having an ordinary skill in the art at the time the invention was made to replace each of the transistors 32, 33, 36, and 37 with a resistor because they are functionally equivalent. Thus, in this modification, the bias circuit (32, 33, 36 and 37) is a passive bias circuit which includes four resistors. Further, as discussed in the above 103 rejection, the advantage of using passive resistor because the impedance of passive resistor inherently is linear (evidence is shown in Col. 5, lines 20-21 of the Stockstad reference, USP 6,429,685; and by Ohm's law V = IR, one skill in the art also recognizes that the passive resistor is linearly).

Applicant also states "Even assuming, *arguendo*, that a resistor is a functional equivalent to a FET, the assertion that they are equivalent is imply not enough to sustain an obviousness rejection under MPEP 2143.01, 2144.06. The Examiner must also provide some suggestion or motivation to combine the references". In response to this argument, the office action clearly states that the advantage of using passive resistor because the impedance of passive resistor inherently is linear (evidence is shown in Col. 5, lines 20-21 of the Stockstad reference, USP 6,429,685; and by Ohm's law V = IR , one skill in the art also recognizes that the passive resistor is linearly).

Applicant also argues that the fundamental premise of the rejection was that Figure. 4(c) of Sasaki indicates that a resistor is equivalent to a field effect transistor that is 'on' state. However, this fundamental premise is incorrect. Sasaki does not teach that a resistor is a functional equivalent to an always-on FET; and applicant also provide various arguments that the resistance model in Sasaki is not a valid resistance model of a FET used in the amplifier of

Zhang. However, this argument is not persuasive because the Sasaki reference clearly teaches that when a transistor is on, it is functionally equivalent to a resistor (see Figure 4c, and Col. 1, lines 21-22 of Sasaki); and because the Zhang reference clearly indicates that transistors 32, 33, 36 and 37 in the amplifier of Zhang remain on during switching (see Col. 7, lines 37-41 of Zhang), so it is valid to construe that each of the transistors 32, 33, 36 and 37 in the amplifier of Zhang functions as a resistor.

Again, applicant also argues that there is no suggestion or motivation in the office action to combine the reference. In response, the office action clearly states that the advantage of using passive resistor in the combination/modification as discussed in the 103 rejection because the impedance of passive resistor inherently is linear (evidence is shown in Col. 5, lines 20-21 of the Stockstad reference, USP 6,429,685; and by Ohm's law V = IR , one skill in the art also recognizes that the passive resistor is linearly).

Applicant also argues that the Stockstad reference serves only to further contrast a FET from a linear resistor and demonstrates the inadequacy of the equivalence model disclosed in Sasaki. In response, the Stockstad reference was cited to support the old and well-known fact that the passive resistor is linear (line 20-21 of Col. 5).

Applicant also states that "while not explicated stated in the record, the Examiner implies that it is well known that an always-on FET is the same as a resistor and, for that reason, there was a motivation to combine Sasaki with Zhang. Pursuant to MPEP 2144.03(c), Applicant hereby challenges this assertion as not properly based upon common knowledge and hereby respectfully requests that the Examiner provide documentary evidence that shows a teaching, suggestion or motivation to combine the cited references". In response, the Sasaki reference

clearly teaches that when a transistor is on, it is functionally equivalent to a resistor (see Figure 4c, and Col. 1, lines 21-22 of Sasaki); and because the Zhang reference clearly indicates that transistors 32, 33, 36 and 37 in the amplifier of Zhang remain on during switching (see Col. 7, lines 37-41 of Zhang), so it is valid to construe that each of the transistors 32, 33, 36 and 37 in the amplifier of Zhang functions as a resistor. Therefore, it is obvious to one having an ordinary skill in the art at the time the invention was made to replace each of the transistors 32, 33, 36, and 37 with a resistor because they are functionally equivalent, and that the advantage of using passive resistor because the impedance of passive resistor inherently is linear (evidence is shown in Col. 5, lines 20-21 of the Stockstad reference, USP 6,429,685; and by Ohm's law V = IR, one skill in the art also recognizes that the passive resistor is linearly).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

February 26, 2004

Long Nguyen
Primary Examiner
Art Unit: 2816
(571) 272-1753